Analysis of Soft-switching Behavior of SiC MOSFET in Phase-shifted Full-bridge Circuits with Different Dead-time for APU

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***Abstract*—The application of SiC power devices in high frequency auxiliary DC converters can greatly improve the power density of the system. The main loss source of phase-shifted full-bridge converters in high frequency operation is the switching loss of devices in APU. It is particularly important for power devices to realize soft-switching. This paper mainly analyses the influence of different dead time on zero voltage switching (ZVS) of phase-shifted full-bridge lagging leg, and obtains the expression of dead time by theoretical calculation. Aiming at the problem of voltage oscillation, the transient equivalent circuit of the device is given, the mathematical model of voltage oscillation is established, the PSIM simulation model is built and tested on a 30 kW phase-shifted full-bridge platform. The simulation and experimental results are in good agreement with the theoretical analysis. The peak voltage oscillation is proportional to the voltage at the front end of the device and the efficiency of the soft-switching converter reaches 97.4%, 1.83% lower than that of hard-switch, which verifies the importance of soft switching.**

Keywords—SiC MOSFET; ZVS; Auxiliary converters; Dead-time; Phase-shifted Full Bridge; Voltage Oscillation.

I. INTRODUCTION

SiC MOSFETs have excellent physical properties such as higher temperature resistance, high voltage blocking ability and faster switching speed [1]. It can improve the switching frequency and the efficiency and power density of the system when applied in phase-shifted full-bridge converter [2]. In the field of rail transit, the application of SiC MOSFET in auxiliary DC converter can improve the efficiency of the system. When switching frequency is high, the volume and weight of transformer and filter can be greatly reduced. However, switching loss becomes the main loss source of the system when SiC MOSFET works at high frequencies. Whether soft switching can be realized is particularly important[3]. For phase-shifted full-bridge circuits, dead-time, load type, and resonant inductance are the key factors affecting ZVS. Reference [4]-[6] analyzed the working state of different dead-time, but did not quantitatively calculate the dead-time range of realizing soft-switching, nor did it analyze the device voltage overshoot, oscillation and system loss under different soft-switching degrees. SiC MOSFET requires stricter dead-time setting, so soft-switching behavior under different dead-time needs to be improved. Modeling and analysis are carried out to provide effective guidance for the application of SiC MOSFET.

In this paper, based on the SiC module CAS300M17BM2 produced by CREE, considering parasitic parameters, the influence of dead-time on phase-shifted full-bridge soft-switching is analyzed. The dead-time range of ZVS can be calculated under different load currents. For SiC MOSFET with different soft-switching degrees, the voltage overshoot and oscillation model is given. The equivalent circuit diagram of the SiC module is shown in Fig. 1.

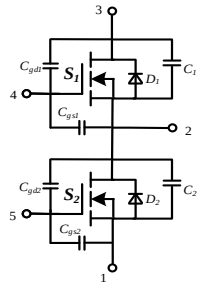


Fig. 1. Equivalent Circuit Diagram Of SiC Module

C_{gd} and C_{gs} are parasitic capacitors, C_1 and C_2 are drain-source capacitors, including C_{oss} of MOSFET and diode junction capacitor, D_1 and D_2 are anti-parallel SBD diodes.

II. EFFECT OF DEAD-TIME ON SWITCHING PROCESS OF LAGGING LEG

A. Prerequisites for Realizing Soft Switching

In phase-shifted full-bridge converter, it is more difficult to realize ZVS by lagging leg than by leading leg. This is because the secondary side of transformer has been short-circuited during the state transition of lagging leg, and the current of primary secondary side does not affect each other[7]. The energy used to realize ZVS is only the energy in resonant inductance L_r. This energy must be satisfied:

$$\frac{1}{2}L_r I_P^2 > \frac{1}{2}C_3 V_{in}^2 + \frac{1}{2}C_4 V_{in}^2 \quad (1)$$

Where, C_3 and C_4 are parasitic capacitors of lagging upper and lower arms.

Equation (1) can be satisfied by increasing the primary current I_p or resonant inductance L_r, but this will lead to a series

of problems such as increased copper consumption and duty cycle loss of transformer[8]. On the premise of satisfactoriness (1), this paper studies the influence of different dead time on soft switching.

B. Transient Switching Process Analysis of Lagging Leg.

Fig. 2 shows the equivalent circuit before S_3 is turned on after S_4 is turned off. Before turning off the S_4, the current flows through the S_4 via the resonant inductor and the diode D_2. When S_4 is turned off, then C_4 starts charging, C_3 starts discharging, and the voltage V_{AB} rises from zero to V_{in}. During this period, the resonant inductance L_r, parasitic capacitance C_3 and C_4 form a resonant cavity [9].

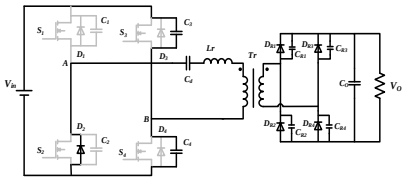


Fig. 2. Transient equivalent circuit after S_4 turned off

At this time, the voltage difference V_{AB} between neutral point voltage of leading leg and neutral point voltage of leading leg can be expressed by (2):

$$v_{BA}(t) = Z_{eq} I_P(t) \sin(\omega t) \tag{2}$$

Where: $\omega = \sqrt{\frac{1}{L_r \cdot 2C}}$, $Z_{eq} = \sqrt{\frac{L_r}{2C}}$, $C_3 = C_4 = C$

Equation (2) shows that the voltage amplitude of V_{BA} is $Z_{eq}I_p$. When v_{BA} (t) = V_{in}, the voltage across C_3 drops to 0. If S_3 is turned on at this time, zero-voltage switching can be realized. Therefore, it is necessary to choose the appropriate dead time to realize the soft switching of the device.

C. The influence of different dead-time on Soft-switching

It can be seen that the voltage across C_3 and V_{BA} are complementary in this process, and the sum of them is V_{in}. In Fig. 3, t_1 represents the turn-off time of the S_4; t_2 represents the time when the voltage across C_3 drops to 0, when v_{BA} (t) = V_{in}; t_3 represents the time when the voltage across C_3 increases from 0 and v_{BA} (t) begins to decrease from V_{in}; t_4 is the time when the V_{C3} rises to V_{in}, and t_{on} is the conduction time of S_3.

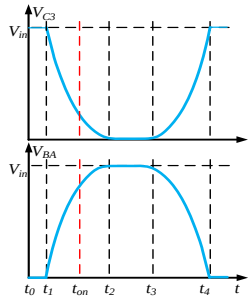
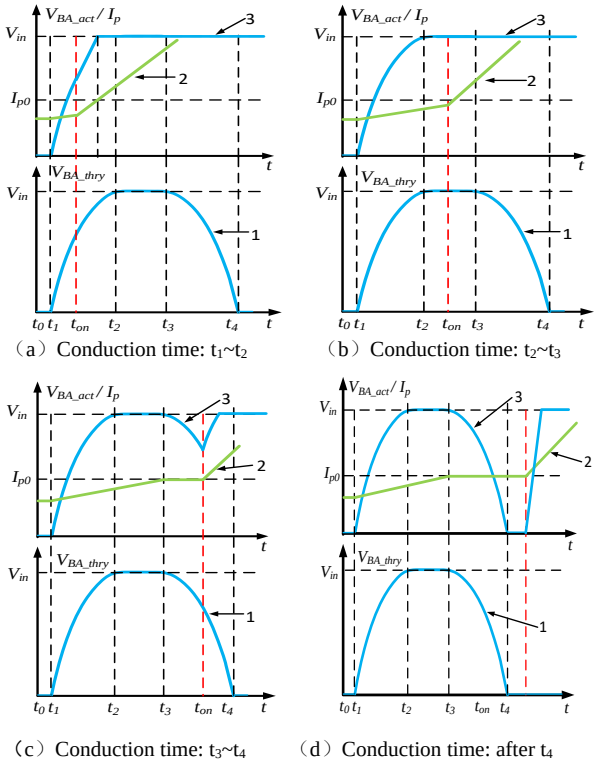


Fig. 3. Variation Curves of the voltage across C_3 and V_{BA} after S_4 turn-off

According to the different turn-on time of S_3, the soft switching state can be divided into four cases. Fig. 4 shows the waveform of V_{BA} and the primary current I_p of transformer corresponding to four different dead time. V_{BA_thry} is the theoretical waveform of neutral-point voltage difference when S_3 is not turned on during the half resonant period after S_4 turn-off; V_{BA_act} is the actual waveform of V_{BA} after S_3 turn-on; I_{p0} is the zero scale of primary side current of transformer, and the current I_p is stable before t_1.



（a）Conduction time: t_1~t_2 （b）Conduction time: t_2~t_3

（c）Conduction time: t_3~t_4 （d）Conduction time: after t_4

Fig. 4. Voltage and current waveforms corresponding to S_3 conduction at different times

- When S_3 is turned on from t_1 to t_2

Before t_{on}, the voltage across C_3 has not been reduced to 0, and the I_p decreases slowly. Under this condition, S_3 is undoubtedly hard conduction. When S_3 is turned on, C_4 is charged by V_{in} via S_3, resulting in fast charging of C_4 to V_{in}, and the I_p acceleration decreases to 0, and increases in reverse.

- When S_3 is turned on from t_2 to t_3

When v_{BA}(t) reaches V_{in} at t_2 and the voltage across S_3 is 0, the ZVS can be realized when S_3 is turned on. Before turning-on of S_3, I_p was in a slow decline state. After S_3 is turned on, the current rapidly decreased to 0 and increased in reverse.

- When S_3 is turned on from t_3 to t_4

From Fig. 4(c), it can be seen that when the I_p decreases to 0 at t_3, L_r cannot continue charging for C_4, the voltage across C_4 decreases, and the voltage across C_3 increases. At this time, V_{AB} decreases from V_{in}, and the voltage across S_3 is no longer 0, so the opening of S_3 is not ZVS.

- When S_3 is turned on after t_4

As can be seen from Fig. 4(d), V_{AB} drops to 0 at t_4, the voltage across of C_3 rises to V_{in}, and S_3 is fully hard-switching.

From the above analysis, it can be concluded that only when S_3 is turned on during t_2-t_3 and the voltage across C_3 is 0, can the zero-voltage switching of S_3 be realized. Therefore, the optimal dead time can only be determined by accurately calculating the corresponding time of t_2 and t_3.

III. Theoretical Calculation Model of Dead Time

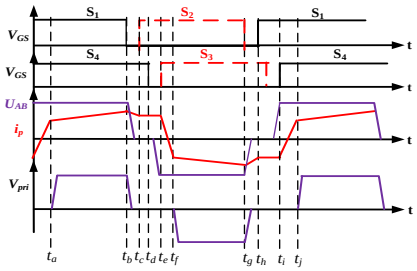


Fig. 5. Principle Diagram of Phase Shift Full Bridge Working Mode

Fig. 5 shows the working principle of the phase-shifted full bridge. At the time of t_a, the duty cycle loss mode of the primary side ends, and the current of the secondary side begins to rise. Therefore, the amplitude of the current of the primary side at t_a is converted to the output current of the secondary side [10]:

$$\begin{cases} I_p(t_a) = n(I_o - \Delta I_o/2) \\ \Delta I_o = \dfrac{nV_{in} - V_o}{L_r}\dfrac{T_s}{2}D_{eff} \\ D_{eff} = V_o/(nV_{in}) \end{cases} \tag{3}$$

Among them, I_o represents output current, V_o represents output voltage, V_{in} is phase-shifted full bridge input voltage, n is transformer ratio, L_r is resonant inductance, $I_o/2$ is output current ripple, D_{eff} is effective duty cycle, T_s is switching period.

During the period from t_a to t_b, because of the short time and the large excitation inductance, the primary current of transformer can be regarded as a linear increase, and the current value at t_b time can be obtained:

$$\begin{cases} I_p(t_b) = I_p(t_a) + I_{Lm} + n\Delta I_o \\ I_{Lm} + n\Delta I_o = \dfrac{T_s V_o}{2nL_m} + \dfrac{(nV_{in} - V_o)V_o T_s}{2L_r V_{in}} \end{cases} \tag{4}$$

L_m is the excitation inductance of transformer.

At t_b, S_1 is turned off and the energy stored in L_r is charged for C_1 and discharged for C_2 respectively. In this process, the primary current I_p decreases in a sinusoidal manner, and the value at t_c is:

$$\begin{aligned} I_P(t_c) &= I_P(t_b)\cos[\arcsin\frac{V_{in}}{Z_{eq}I_P(t_b)}] \\ &= \frac{\sqrt{Z_{eq}^2 I_P(t_b)^2 - V_{in}^2}}{Z_{eq}} \end{aligned} \tag{5}$$

During the period from t_c to t_d, S_2 and S_4 are all in conducting state, and the original side of transformer is in the continuous current state. The current in this stage can be regarded as unchanged.

$$I_p(t_d) = I_p(t_c) \tag{6}$$

The t_c to t_d period in Fig. 5 correspond to the t_0 to t_1 period in Fig. 4(d). The current at t_d in Fig. 6 is the current at t_1 in Fig. 4(d). In order to facilitate the calculation of dead time, the wiring is derived based on the timing in Fig. 4.

The energy in L_r is discharged and charged to C_3 and C_4 respectively via D_2 when S_4 is turned off at t_1. At this time, the equivalent circuit fig.3 can be obtained as follows:

$$2C\frac{dV_{C4}(t)}{dt} = I_p(t) \tag{7}$$

$$L_r\frac{dI_p(t)}{dt} + V_{C4}(t) = 0 \tag{8}$$

It is easy to know that the voltage across C_4 is $v_{BA}(t)$, which can be obtained as follows:

$$v_{BA}(t) = V_{C4}(t) = Z_{eq}I_P(t_1)\sin(\omega(t - t_1)) \tag{9}$$

$$I_p(t) = I_p(t_1)\cos(\omega(t - t_1)) \tag{10}$$

At t_2, the voltage of $v_{BA}(t)$ rises to V_{in}, and the time from t_1 to t_2 can be expressed as (11):

$$t_{12} = \frac{1}{\omega}\arcsin\left(\frac{V_{in}}{Z_{eq}I_p(t_1)}\right) \tag{11}$$

After t_2, the bus voltage is directly added to the resonant inductor, and the current I_p of the original side decreases linearly from t_2.

$$I_p(t) = I_p(t_2) - \frac{V_{in}}{L_r}(t - t_2) \tag{12}$$

$I_p(t_2)$ is the primary current at t_2. By the time of t_3, the current of the original side is reduced to zero, and the duration of this state is as follows:

$$t_{23} = \frac{L_r I_p(t_2)}{V_{in}} \tag{13}$$

According to (9) ~ (13), an analytical model of the maximum time range of soft switching with respect to load current can be obtained:

$$t_{23} = \frac{L_r \cdot I_p(t_1)\cos\left(\arcsin\left(\dfrac{V_{in}}{Z_{eq}I_p(t_1)}\right)\right)}{V_{in}} \tag{14}$$

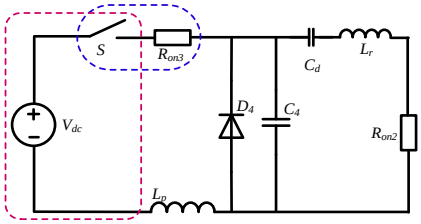
Dead-time settings need to satisfy the relationships:

$$t_{12} < t_{dt} < t_{12} + t_{23} \tag{15}$$

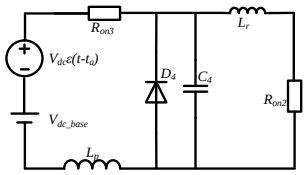
IV. Modeling of SiC MOSFET Switching Behavior

Due to parasitic capacitance and inductance of the device and the circuit, when the device is in a nonsoft-switching state, it will lead to voltage oscillation , which will increase the voltage stress of the device. Therefore, it is necessary to model the switching behavior of SiC MOSFET to analyze the oscillation at different soft-switching levels. Because SiC MOSFET has fast turn-on speed and on-resistance, it can be regarded as a

series connection of ideal switch and on-resistance. A phase-shifted full-bridge transient equivalent model considering parasitic parameters of devices is obtained as shown in Fig. 6(a). R_{on} is the on-resistance of corresponding devices, L_p is the parasitic inductance of circuits, and the initial voltage of devices is different under different soft-switching degrees. The voltage source is equivalent to the series connection of the basic voltage source and step voltage source, in which the C_d value is larger and plays a direct role in the circuit. It can be regarded as a short circuit in the transient state. The simplified equivalent circuit is shown in Fig. 6 (b).



(a) Equivalent model considering parasitic parameters



(b) Simplified equivalent model

Fig. 6. Transient Equivalent Model of Device S_3 Conduction

The voltage V_{S4} across S_4 (C_4) in complex frequency domain can be obtained from Fig. 6 (b):

$$V_{S4}=\frac{\left(V_{dc\_base}+\frac{V_{dc}}{s}\right)\bullet\left(sL_r+R_{on2}\right)//\frac{1}{sC_4}}{\left(sL_r+R_{on2}\right)//\frac{1}{sC_4}+R_{on3}+sL_p} \tag{16}$$

After expansion, we can get:

$$V_{S4}=\frac{\left(V_{dc\_base}+\frac{V_{dc}}{s}\right)\bullet\left(sL_r+R_{on2}\right)}{\begin{pmatrix}s^3\left(L_rL_pC_4\right)+s^2\left(L_rC_4R_{on3}+L_pC_4R_{on2}\right)+\\ s\left(L_r+L_p+C_4R_{on2}R_{on3}\right)+\left(R_{on2}+R_{on3}\right)\end{pmatrix}} \tag{17}$$

Because the resonant inductance value L_r is large, dividing (17) up and down by L_r and eliminating the denominator of L_r, the simplification can be obtained:

$$V_{S4}=\frac{V_{dc\_base}+\frac{V_{dc}}{s}}{s^2L_pC_4+sC_4R_{on3}+1} \tag{18}$$

The expression of formula (19) in time domain can be obtained by inverse Laplacian transformation:

$$V_{S4}=\left(V_{dc\_base}+V_{dc}\right)+\frac{V_{dc}}{\sqrt{\omega^2L_pC_4}}\bullet e^{\alpha t}\sin\left(\omega\left(t\text{-}t_a\right)\right) \tag{19}$$

$$\begin{cases}\omega=\sqrt{\frac{1}{L_pC_4}-\frac{R_{on3}^{\ 2}}{4L_p^{\ 2}}}\\ \alpha=-\frac{R_{on3}}{2L_p}\end{cases} \tag{20}$$

According to (18) (19), the peak voltage oscillation can be obtained:

$$V_{S4,max}=\left(V_{dc\_base}+V_{dc}\right)+\frac{V_{dc}}{\omega^2L_pC_4}\bullet e^{-\alpha t_p}\sin\left(\omega t_p\right) \tag{21}$$

$$t_p=\frac{1}{\omega}\arctan\left(-\frac{\omega}{\alpha}\right) \tag{22}$$

It can be seen from (21) that the maximum voltage is related to the initial value of voltage across the device before it is turned on, the peak value of voltage overshoot is proportional to the V_{dc}, and V_{dc} is related to the degree of soft switching of the device.

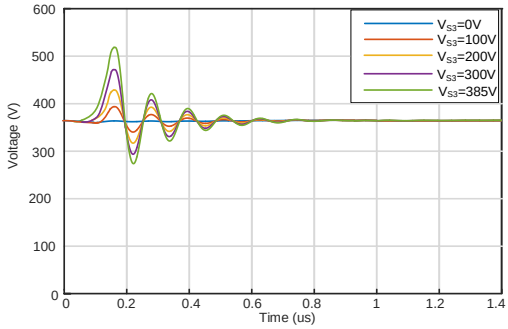


Fig. 7. Variation of Over-shoot Voltage with Soft Switching Degree

Through matlab simulation, the voltage oscillation contrast waveforms of S_3 at different initial voltages are obtained. It can be seen from Fig. 7, in the state of fully soft switching, the device voltage does not oscillate, which is consistent with the theoretical analysis. Besides the higher the voltage across the power device is, the more serious the voltage oscillation is.

V. Simulation and Experimental Results

TABLE I. System Hardware Parameter

Parameter	Table Column Head		
	symbol	***value***	***unit***
Input voltage	V_{in}	375	V
Resonant inductor	L_r	7.2	uH
Output capacitance	C	2.5	nF
Transformer Ratio	n	1:1.68	----
Isolating capacitor	C_d	30	uF
Load resistance	R_d	5	Ω

TABLE I. is the hardware parameter table of the system, which can be used to deduce the dead time. Equation (3) ~ (6) can be used to calculate that the original current I_p after switching off S_4, which is about 49.82A.. Taking this value into (10) - (14), we can calculate that:

$$t_{12} = \frac{1}{\omega}\arcsin\left(\frac{V_{in}}{Z_{eq}I_p(t)}\right) = 42\text{ns}$$

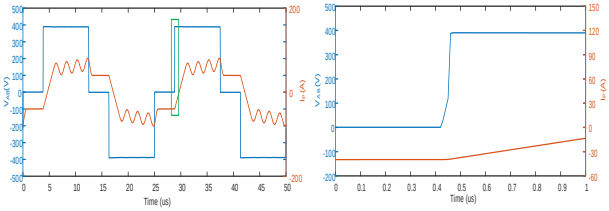
$$t_{23} = \frac{L_t I_p(t_2)}{V_{in}} = 928\text{ns}$$

Therefore, it can be seen from (15) that the dead time should be chosen:

$$42\text{ns} < t_{dt} < 970\text{ns}$$

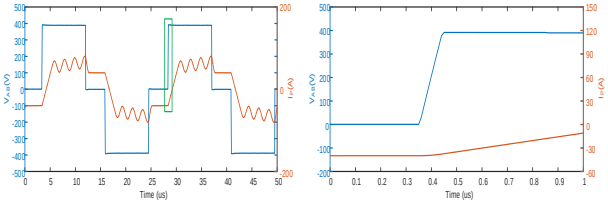
A. *Simulation Verification of Different Dead-time*

Four dead-time intervals of 30ns, 500ns, 1000s and 1200ns are selected to simulate and verify the theoretical analysis, and the reliability of their application in practice is verified by PSIM simulation. For each of the following pictures, the right one is the enlarged part of the left one.



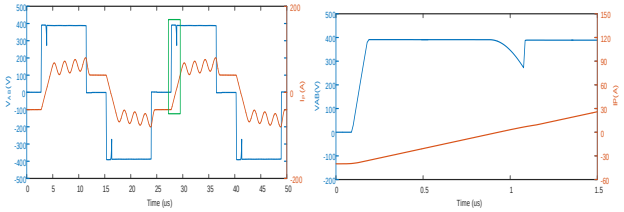
(a) Overall (b) Local

Fig. 8. V_{BA} and primary current I_p waveforms with t_d= 30ns



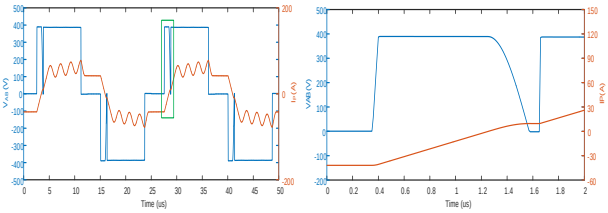
(a) Overall (b) Local

Fig. 9. V_{BA} and primary current I_p waveforms with t_d= 500ns



(a) Overall (b) Local

Fig. 10. V_{BA} and primary current I_p waveforms with t_d= 1000s



(a) Overall (b) Local

Fig. 11. V_{BA} and primary current I_p waveforms with t_d= 1200ns

From Fig. 8 to Fig. 11, it can be found that the simulation results are in good agreement with the theoretical analysis in Part III.

B. *Experimental Verification of Different Dead-time*

The test prototype is a DC/DC converter in the all SiC auxiliary power supply system for subway. The characteristic of this system is that all power devices are SiC devices. The phase-shifted full bridge topology isolated by high frequency transformer is adopted. The experiment power is 30 kW and the switching frequency of power devices is 40 kHz. The physical drawings of the test prototype are as follows:

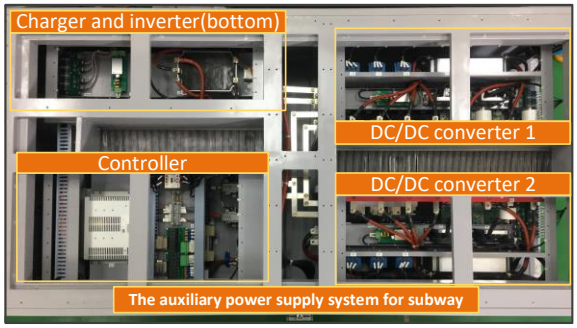
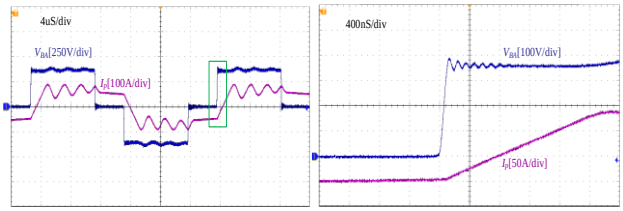


Fig. 12. *Experimental platform*

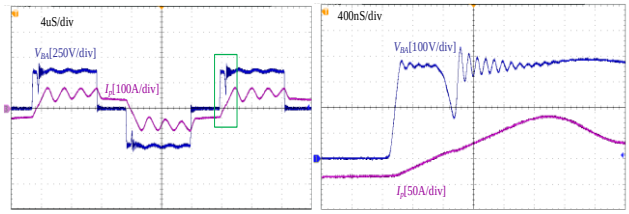
Because the minimum dead time of SiC MOSFET driver is 250ns, the experiment corresponding to 30ns cannot be carried out, so it is ignored.



(a) Overall (b) Local

Fig. 13. V_{BA} and primary current I_p waveforms with t_d= 500ns

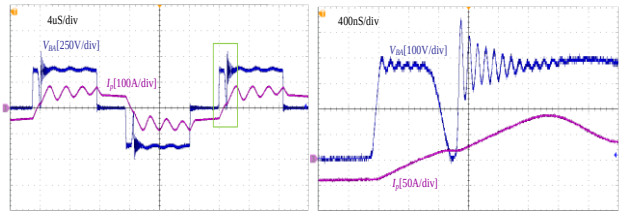
It can be seen from Fig. 13 that the device can realize soft switching. Under this experimental condition, the output power is 28.28 kW and the system efficiency can reach 97.4%.



(a) Overall (b) Local

Fig. 14. V_{BA} and primary current I_p waveforms with t_d= 1000ns

It can be seen from Fig. 14 that the switching state of the device under this condition is hard switch. The voltage across the device is about $V_{in}/2$ before turning on, and the system efficiency is 96.88%. Under this condition, the efficiency decreases by 0.52% compared with that of soft-switching.



(a) Overall (b) Local

Fig. 15. V_{BA} and primary current I_p waveforms with t_d= 1200ns

It can be seen from Fig. 15 that the switching state of the device under this condition is completely hard-switching, and the voltage across the device is V_{in} before switching on. Under this condition, the system efficiency is 95.57%. At this time, the efficiency decreases by 1.83% compared with that of soft switching. Besides, we can be see that the amplitude of voltage oscillation is the largest. Comparing with Fig. 13 and Fig. 14, it can be found that the amplitude of voltage oscillation increases with the decrease of soft switching degree. When the device is completely hard-switching, the voltage stress of the device will increase and the reliability of the system will be reduced.

Fig. 16 shows that the maximum overshoot voltage across S_4 increases with the decrease of the soft switching degree. Without soft switching, the maximum voltage stress of S_4 is about 550V. The peak value of the actual measured overvoltage (red circle o) is slightly smaller than the theoretical value. It can be seen that the simplification of the model is reasonable. It is also proved that the voltage oscillation is caused by parasitic capacitance and stray inductance resonance. The oscillation frequency has little relationship with resonant inductance L_r and isolating capacitance C_d.

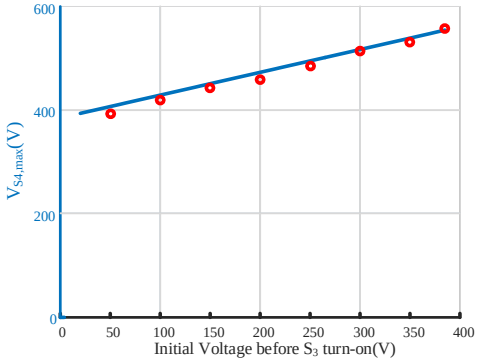


Fig. 16. Variation of Over-shoot Voltage with Soft Switching Degree

Through simulation and experimental waveforms, it can be found that the current oscillates greatly in Fig. 14-16. This is due to the resonance of resonant inductance, transformer leakage inductance and rectifier junction capacitance during the circulating current, which causes the current oscillation [11], which is not discussed here.

VI. Conclusion

Through the analysis of the basic working principle of phase-shifted full bridge, the dead-time limits of soft-switching are deduced theoretically, and four typical working conditions corresponding to different dead-time are determined. The simulation are carried out by PSIM simulation software, which verify the different effects of different dead-time on soft-switching in 30ns, 500ns, 1000ns and 1200ns. The voltage V_{AB} and primary side current I_p waveforms of Transformer under three dead-time conditions were tested by prototype experiments, and the corresponding system efficiency was measured. Through comparison, it is found that the experimental results and simulation results are in agreement with the theoretical analysis, but the voltage oscillation will become more serious with the deepening of the hard switching. It is found that the peak value of voltage oscillation is proportional to the voltage across the device before turning on, and the oscillation period remains unchanged. Finally, the system losses under different soft-switching degrees are compared. The system efficiency is 97.4% at the condition of zero-voltage switching. With the decrease of soft-switching degree, the system efficiency becomes higher and higher. The efficiency of full hard-switching is 1.83% lower than that of zero-voltage switching. The importance of phase-shifted full-bridge soft-switching is verified, which provides theoretical and experimental guidance for the application of SiC MOSFET in practical circuits.

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