Design and Implementation of Wireless Power Transfer Systems with Improved Capacitor Error Tolerance

Yi Wang, *Student Member*, *IEEE*, Zhongping Yang, *Member*, *IEEE*, and Fei Lin, *Member*, *IEEE*

***Abstract*—Owing to manufacturing defects and aging, compensation capacitors are inevitably prone to errors, leading to the performance deprecation in a wireless power transfer (WPT) system. This paper focuses on the sensitivity analysis of system characteristics to capacitor errors and design methods to improve detuning tolerance. First, the output voltage, power factor, transfer efficiency, and capacitor voltages are derived for LCC-S compensated WPT systems. The worst-case scenarios (i.e., the maximum and minimum values of these indicators) are used to evaluate the effect of capacitor errors. They are calculated under detuned conditions with different inverter quality factors, load quality factors, and the ratios of the primary coil's self-inductance to the compensation inductance. Then, the design constraints are summarized to meet the system requirements considering ±10% capacitor errors. A simplified and easy-to-follow system design process is proposed and a 22-kW wireless charger for an electric bus is designed. Experimental results show that, compared with the traditional design, the change ratio of the output voltage of the proposed design is reduced from between -40.9% and 13.1% to between -21.5% and 12.4%. The lowest power factor is increased from 0.64 to 0.78, and the maximum drop in transfer efficiency is reduced from 9.9% to 5.9%.**

***Index Terms*—Capacitor errors, detuning tolerance, quality factor, wireless power transfer (WPT).**

NOMENCLATURE

U_P	Output voltage of the primary inverter
U_S	Output voltage of the coupling coils
U_O	Output voltage of the secondary rectifier
L_P	Self-inductance of the primary coil
L_S	Self-inductance of the secondary coil
M	Mutual inductance of the coupling coils
L_r	Primary series compensation inductance
G_V	Voltage gain
C_r	Actual primary parallel compensation capacitance
C_P	Actual primary series compensation capacitance
C_S	Actual secondary series compensation capacitance
R_r	Resistance of primary series compensation inductor
R_P	Resistance of primary coil
R_S	Resistance of secondary coil
R_E	Equivalent load resistance of the coupling coils.
ω	Angular frequency
Z_P	Impedance after the primary parallel compensation capacitor
Z_S	Sum of the impedance of secondary coil and series compensation capacitor
Z_{in}	Load impedance of the primary inverter
Q_{in}	Primary inverter quality factor
Q_O	Load quality factor
L_{PR}	The ratio of the primary coil's self-inductance to the primary compensation inductance
Q_r	Quality factor of the primary compensation inductor
Q_P	Quality factor of the primary coil
Q_S	Quality factor of the secondary coil
P_{in}	Input power of the coupling coils
P_O	Output power the coupling coils
η_{coup}	Transfer efficiency from the primary inverter output to the secondary rectifier input
η_{sys}	System transfer efficiency from the grid input to the secondary rectifier output
$C_{r\text{-}0}$	Ideal primary parallel compensation capacitance
$C_{P\text{-}0}$	Ideal primary series compensation capacitance
$C_{S\text{-}0}$	Ideal secondary series compensation capacitance
$U_{S\text{-}0}$	Ideal output voltage the coupling coils
U_{S_Max}	Maximum output voltage with compensation errors
U_{S_Min}	Minimum output voltage with compensation errors
λ	Power factor of the primary inverter
U_{C_r}	Voltage of primary parallel compensation capacitor
$U_{C_{r\text{-}0}}$	Ideal voltage of primary parallel compensation capacitor
U_{C_P}	Voltage of primary series compensation capacitor
$U_{C_{P\text{-}0}}$	Ideal voltage of primary series compensation capacitor
U_{C_S}	Voltage of secondary series compensation capacitor
$U_{C_{S\text{-}0}}$	Ideal voltage of secondary series compensation capacitor
k	Coupling coefficient
$Q_{in\text{-}s}$	Starting point of Q_{in} in the design phase
$Q_{O\text{-}s}$	Starting point of Q_O in the design phase
$L_{PR\text{-}s}$	Starting point of L_{PR} in the design phase

This work was supported by the Fundamental Research Funds for the Central Universities of China under Grant 2020YJS157.

Y. Wang, Z. Yang and F. Lin are with the School of electrical engineering, Beijing Jiaotong University, Beijing, 100044, China (e-mail: 16121534@bjtu.edu.cn; zhpyang@bjtu.edu.cn; flin@bjtu.edu.cn). (corresponding author: Fei Lin; +86-010-5168-4029; e-mail: flin @bjtu.edu.cn).

I. Introduction

Wireless power transfer (WPT) technology has attracted widespread attention as an effective alternative to the traditional plug-in power transfer method with cables and has been widely studied in the last 30 years. Using electromagnetic induction, a WPT system would naturally have some unique benefits, such as convenience, safety, and weather proof [1]. These advantages make WPT become an attractive power solution for various applications, like home and consumer electronics [2], medical implants [3], and electric vehicles [4].

A WPT system consists of a primary transmitting coil, a secondary receiving coil, and power converters. The coupling coefficient of the coupling coils is relatively low compared to that of a traditional transformer, generally 0.01–0.5 [5]. Therefore, a compensation circuit is needed to reduce the reactive power, thereby improving the transfer efficiency. Capacitors are necessary for compensation circuits that usually resonate with coils at the working frequency, which gives the WPT system some appealing characteristics. For example, the ideally compensated WPT system with the SS topology has a constant output current, which is suitable for charging batteries.

The performance of the WPT system is usually analyzed when the perfect resonance is achieved, which is the premise for the excellent characteristics of a compensation topology. However, in practice, there will be errors in compensation capacitors. The commercial capacitors that are currently in use usually have several levels of accuracy, for example, ± 10%, ± 5%, and so on. The aging of the capacitors and the increase in the temperature induce changes in the capacitances [6]. These capacitor errors are determined by the inherent characteristics of the capacitors, and cannot be avoided. Consequently, imperfect compensation, rather than ideal compensation, is the norm for a WPT system. The reactive power of a detuned WPT system may not be neglected, so the capacity of the primary converter needs to be increased, which undoubtedly increases the cost. What is more, the original transfer characteristics cannot be maintained, resulting in failure to meet the load demand. Since the resonant condition is lost, components in the circuit may suffer greater electrical stress than the rated values, which may cause safety problems. So, it is imperative to analyze the performance of the WPT system when compensation errors exist and then take some measures to minimize the effect of capacitor errors on the system.

Some researchers have studied the effect of parameter variations on the system performance. Wang *et al.* [7] studied how the input impedance angle changed with the load resistance when there was a compensation error. They changed only one parameter at a time. The effect of the inductance variations on the double-sided *LC*-compensated capacitive power transfer system's frequency property was studied in [8]. Lu *et al.* [9] simulated the output power and efficiency sensitivity to circuit parameter variations in the double-sided LCC-compensated WPT system using LTspice software. However, only a limited combination of parameter variations was analyzed in [8], [9]. In addition, all the above studies are based on the determined coil parameters. These studies focused only on the effect of parameter variations on the system, but did not discuss the influence of circuit parameters on the sensitivity and solutions of improving the system's tolerance to component errors.

The design of coupling coils is also very important due to their decisive roles in the performance of a WPT system. Some design methods are proposed in [10]-[15], which usually aim to obtain the coupling coils with high transfer efficiency, high power density, and good misalignment tolerance. Since the effect of capacitor errors on the system performance is not analyzed in detail, capacitor error tolerance is not taken into consideration in these design methods.

To improve the capacitor error tolerance of the WPT system, this paper analyzes the impacts of capacitor errors on the system performance in detail and then proposes an easy-to-follow design process to obtain a high detuning-tolerant system. The LCC-S compensation topology is selected because it has good constant voltage output characteristics. Three design variables, i.e., the inverter quality factor, the load quality factor, and the ratio of the primary coil's self-inductance to the primary compensation inductance, are defined and used to derive the transfer characteristics of the WPT system, which simplify the analysis of the relationship among transfer characteristics with system parameters and capacitor errors. Since capacitor errors are unpredictable and inevitable, this paper uses numerical method and bottom-line thinking to analyze the sensitivity of the system performance to compensation errors with three compensation capacitor errors considered simultaneously. The guidelines of the system design are then developed to improve the detuning tolerance based on the optimization of the above three design variables, which would finally help the design of the whole system.

This article is organized as follows. In Section II, the transfer characteristics of the WPT system are evaluated with the output voltage, power factor, transfer efficiency, and compensation capacitors' terminal voltages, with capacitor errors considered. Section III proposes a simplified and easy-to-follow design process. A 22-kW WPT system with high detuning tolerance is designed and implemented with the proposed design process in Section IV. The experimental results prove the validity of the theoretical analysis and the effectiveness of the proposed design method. Finally, Section V concludes this article.

II. WPT System with Compensation Errors

A. System Configuration

Fig.1 shows the power supply schematic of an LCC-S compensated WPT system.

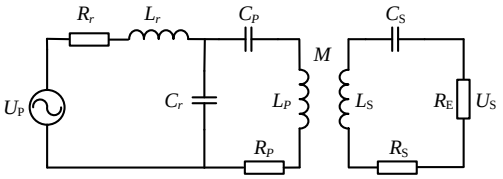

Fig. 1. Typical schematic diagram of an LCC-S compensation topology.

According to Kirchhoff's voltage law, the output voltage can be obtained as follows [16], [17]:

$$U_S = \frac{\omega M R_E U_P}{|(Z_S+R_E)[(1-\omega^2 L_r C_r + j\omega C_r R_r)Z_P + j\omega L_r + R_r]|} \quad (1)$$

where

$$Z_P = \frac{\omega^2 M^2}{Z_S+R_E} + j\omega L_P + R_P + \frac{1}{j\omega C_P} \quad (2)$$

$$Z_S = j\omega L_S + R_S + \frac{1}{j\omega C_S} \quad (3)$$

In the actual system, the parasitic resistances of coils and compensation inductor are small, which satisfy the following formula and could be neglected:

$$\omega L_r, \omega L_P, \omega L_S, R_E \gg R_r, R_P, R_S \quad (4)$$

When the compensation parameters satisfy the below equation

$$\omega L_r = \frac{1}{\omega C_r} = \omega L_P - \frac{1}{\omega C_P}, \omega L_S = \frac{1}{\omega C_S} \quad (5)$$

then the output voltage can be rewritten as

$$U_S = \frac{M}{L_r} U_P \quad (6)$$

That is, the voltage gain G_V is equal to M/L_r. The load impedance of the primary inverter is expressed as follows:

$$Z_{in} = j\omega L_r + R_r + \frac{Z_P}{1+j\omega C_r Z_P} \quad (7)$$

A higher power factor allows the inverter to output less reactive power with less inverter and line loss, so zero phase angle (ZPA) for the primary inverter is required. With the compensation parameters shown in (5), ZPA is achieved and (7) could be expressed as follows with parasitic resistances neglected:

$$Z_{in} = \frac{L_r^2}{M^2} R_E \quad (8)$$

According to (6) and (8), for given coupling coils, the output voltage can be set to any desired value to some extent by changing the compensation inductance and the corresponding compensation parameters, which also means that the output power can be adjusted arbitrarily within a certain range with ZPA. An added degree of freedom makes the system design simple; however, if the system characteristics are not analyzed comprehensively and accurately, the obtained system may perform poorly in some aspects, such as detuning tolerance.

The quality factor is defined as the ratio of reactive to real power in [5], and the primary inverter quality factor Q_{in} and load quality factor Q_O with perfect compensation could be expressed

$$Q_{in} = \frac{\omega L_r}{Z_{in}} = \frac{\omega M^2}{L_r R_E}, Q_O = \frac{\omega L_S}{R_E} \quad (9)$$

The quality factors of the compensation inductor and the primary and secondary coils are obtained, respectively, as

$$Q_r = \frac{\omega L_r}{R_r}, Q_P = \frac{\omega L_P}{R_P}, Q_S = \frac{\omega L_S}{R_S} \quad (10)$$

Combined with (5), (9), and (10), the expressions of output voltage and load impedance (1) and (7), respectively, are rewritten as

$$U_S = \frac{M U_P}{L_r} \frac{1}{\left|\frac{Q_{in}}{Q_r} + \left(1+\frac{Q_O}{Q_S}\right)\left(\frac{L_{PR}}{jQ_P Q_r}+1\right)\right|} \quad (11)$$

$$Z_{in} = j\omega L_r \left[1 - \frac{j}{Q_r} + \frac{1}{-1+\frac{1}{\frac{Q_{in}}{j\left(1+\frac{Q_Q}{Q_S}\right)}+1-\frac{jL_{PR}}{Q_P}}}\right] \quad (12)$$

The transfer efficiency from the primary inverter output to the secondary rectifier input can then be calculated using the following formula:

$$\eta_{coup} = \frac{P_O}{P_{in}} = \frac{\frac{U_S^2}{R_E}}{\mathrm{Re}\left[\frac{U_P^2}{Z_{in}}\right]} = \frac{\frac{Q_{in}}{\left|\frac{Q_{in}}{Q_r}+\left(1+\frac{Q_O}{Q_S}\right)\left(\frac{L_{PR}}{jQ_P Q_r}+1\right)\right|^2}}{\mathrm{Re}\left[\frac{1}{j+\frac{1}{Q_r}+\frac{j}{-1+\frac{1}{\frac{Q_{in}}{j\left(1+\frac{Q_Q}{Q_S}\right)}+1-\frac{jL_{PR}}{Q_P}}}}\right]} \quad (13)$$

Here, Re[] is the real part of the value in brackets.

B. Effect of Compensation Errors on the Transfer Characteristics

Non-ideal compensation is mainly caused by errors in the passive elements. For an LCC-S compensated WPT system, they are L_r, L_P, L_S, C_r, C_P, and C_S. Compared with the capacitors, the coupling coils and the compensation inductor can be manufactured with higher accuracy by using molds and adjusting the air gap (specifically for the compensation inductor). Generally, inductors do not have an aging problem, and the temperature has little effect on the inductance. However, a capacitor will be considered effective before the relative deviation of the actual capacitance value exceeds 10% [6]. As a result, the capacitances of the capacitors are more easily affected compared with coils' inductance, leading to greater errors in practical applications. So, in the following, only the capacitor errors are discussed, whereas the others are considered to be the designed values, which could help reduce the difficulty of analysis while maintaining high accuracy.

Here, k_r, k_P, and k_S are used to express the relationship between actual capacitances C_r, C_P, and C_S and the ideal capacitances calculated by (5), that is, $C_{r\text{-}0}$, $C_{P\text{-}0}$, and $C_{S\text{-}0}$:

$$C_r = k_r C_{r-0}, C_P = k_P C_{P-0}, C_S = k_S C_{S-0} \quad (14)$$

For a WPT system, a stable and controllable output voltage is desired. According to the above analysis, the output voltage of an ideally compensated condition is equal to $M \cdot U_P/L_r$. However, when compensation errors exist, it is difficult to know, without a detailed analysis, how the output voltage changes. Besides, a high power factor and high transfer efficiency are required. Therefore, the changes in the output voltage, power factor, and transfer efficiency will be analyzed in detail when compensation errors exist. Meantime, if the voltages and currents of the compensation capacitors change significantly, they may exceed the safety margin and cause safety problems. Therefore, the electrical stress of the compensation capacitors will also be analyzed in the following sections.

1) *Output Voltage*

The output voltage with all parasitic resistances neglected is obtained after substituting (14) into (1) and combining (5), (9), and (10). The ratio of the output voltage with the compensation errors to that of the ideally compensated condition is used to evaluate the effect of compensation errors on the output voltage, that is,

$$\frac{U_S}{U_{S-0}} = \frac{1}{\left|(1+jaQ_O)\left[(1-k_r)\left(\frac{Q_{in}}{j-aQ_O}+b\right)+1\right]\right|} \quad (15)$$

where,

$$a = 1 - \frac{1}{k_S}, b = L_{PR}\left(1-\frac{1}{k_P}\right) + \frac{1}{k_P} \quad (16)$$

Since the input voltage and the compensation inductance generally do not change, it can be seen from (6) that the output voltage is a constant with perfect compensation in theory when the mutual inductance is kept unchanged. However, the output

voltage amplitude becomes a function of (Q_{in}, Q_O, L_{PR}, k_r, k_P, k_S) for imperfect compensation, which is a 6-D problem and makes the theoretical analysis difficult. It should be mentioned that the inverter quality factor and load quality factor may change when there are compensation errors, but Q_{in} and Q_O in (15) are still calculated by (9), which are the values of the perfect compensation condition. These six parameters could be divided into two types. The errors of three compensation capacitors, (k_r, k_P, k_S), are unavoidable and unpredictable, which may dramatically degrade the system performance at some values. The other three parameters, (Q_{in}, Q_O, L_{PR}), are determined by the coupling coils, compensation inductance, and load, which could be optimized during the design phase by following some principles to reduce the sensitivity on compensation errors. So, the main work next is to study the effect of (Q_{in}, Q_O, L_{PR}) on the system's sensitivity to compensation errors, and then determine the design constraints for a reasonable system.

The capacitor errors have different levels, and small errors mean high costs, in general. It is assumed that the errors of the actual capacitances do not exceed ± 10%, that is, $0.9 \le k_r, k_P, k_S \le 1.1$. This assumption is reasonable and representative considering that the capacitances will change with temperature and time. To accurately and comprehensively assess the effect of (Q_{in}, Q_O, L_{PR}) on the system's sensitivity to compensation errors, the worst case should be studied for different combinations of (Q_{in}, Q_O, L_{PR}) as (k_r, k_P, k_S) are unavoidable and unpredictable. For the output voltage, the worst-case scenario means that the ratio of the output voltage of the detuned condition to that of the ideal compensation condition, $U_S/U_{S\text{-}0}$, has reached its maximum or minimum. From (15), accurate analytical solutions can be obtained to calculate the maximum and minimum values through mathematical calculations, but it is rather complicated and cumbersome as this is a 6-D problem. Alternatively, a numerical methodology is used. So, an iterative process is used here over a practical range of Q_{in} and Q_O from 0.5 to 10 and L_{PR} from 1 to 15, and a nonlinear programming function is applied to calculate the maximum and minimum output voltages of each combination of (Q_{in}, Q_O, L_{PR}). The maximum and minimum ratios of the output voltage between detuned condition and ideal compensation condition are plotted as shown in Fig. 2. For ease of graphic visualization, only the pictures when L_{PR}=3 and 12 are shown. The effect of L_{PR} on the system is gradual, that is, the color of the images gradually changes in the direction of increasing or decreasing the value as the L_{PR} increases. So, showing two values of L_{PR} is enough.

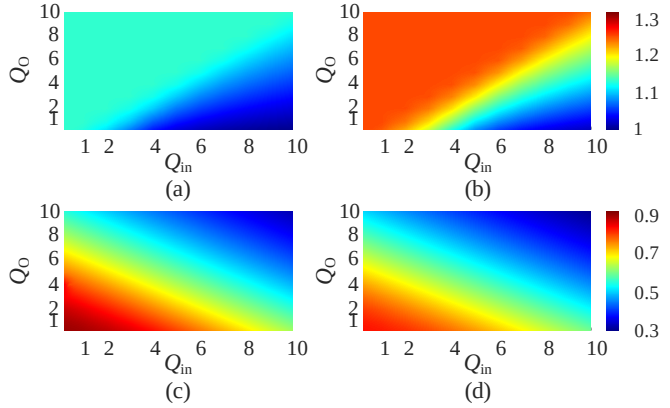

Fig. 2. Variations of the maximum and minimum ratios of the output voltage of detuned condition to that of ideal compensation condition with Q_{in}, Q_O, and L_{PR}. Maximum change ratio when (a) L_{PR}=3 and (b) L_{PR}=12. Minimum change ratio when (c) L_{PR}=3 and (d) L_{PR}=12.

It is worth mentioning that the maximum value usually happens when (k_r, k_P, k_S) is equal to (1.1, 1.1, 0.9), whereas the minimum value generally happens at (0.9, 1.1, 0.9).

According to Fig.2, the increase in Q_{in} is beneficial to reduce U_{S_Max}, but also reduces U_{S_Min}, so Q_{in} should be compromised, whereas Q_O should be small as increasing Q_O will increase U_{S_Max} and decrease U_{S_Min}. Besides, increasing L_{PR} will increase U_{S_Max}, but has a little effect on U_{S_Min}. As a result, L_{PR} should be as small as possible.

2) *Power factor*

When the compensation errors exist, the load impedance of the inverter is derived as follows:

$$Z_{in} = j\omega L_r + \frac{j\omega L_r}{-k_r + \frac{1}{\frac{Q_{in}}{j-aQ_O}+b}} \tag{17}$$

The power factor can be calculated by

$$\lambda = \frac{\mathrm{Re}[Z_{in}]}{|Z_{in}|} \tag{18}$$

Here, the influence of (Q_{in}, Q_O, L_{PR}) on the minimum power factor is analyzed only as the maximum is 1. The variation of the minimum power factor with (Q_{in}, Q_O, L_{PR}) is drawn as Fig.3.

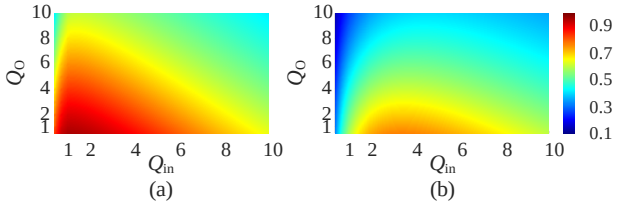

Fig. 3. Variation of the minimum power factor with Q_{in}, Q_O, and L_{PR}. (a) L_{PR}=3. (b) L_{PR}=12.

The minimum power factor is likely to occur when (k_r, k_P, k_S) is equal to (1.1, 0.9, 1.1) and happens at (0.9, 1.1, 0.9) at some combinations of (Q_{in}, Q_O, L_{PR}). From the color change trend of the images, it can be found that when L_{PR} is large, the power factor is less than 0.7 in more areas. The power factor increases first and then decreases as Q_{in} increases, and the turning point increases with increasing L_{PR}. For Q_O, its reduction is good for improving the power factor. Therefore, lower Q_O and lower L_{PR} are wanted to maintain a high power factor, whereas Q_{in} should be compromised.

3) *Transfer Efficiency*

The transfer efficiency is the most important index for a WPT system, so the variations in transfer efficiency with capacitor errors considered are also analyzed here. When the capacitor errors are considered, the transfer efficiency from the primary inverter output to the secondary rectifier input, η_{coup}, is modified from (13) to

$$\eta_{coup} = \frac{Q_{in}}{\frac{\left|c\left(\left(1-k_r+\frac{jk_r}{Q_r}\right)\left(\frac{Q_{in}}{jc}+b'\right)+1+\frac{1}{jQ_r}\right)\right|^2}{\mathrm{Re}\left[\frac{1}{j+\frac{1}{Q_r}+\frac{j}{-k_r+\frac{1}{\frac{Q_{in}}{jc}+b'}}}\right]}} \tag{19}$$

where,

$$b'=b+\frac{L_{PR}}{jQ_P}, c=1+\frac{Q_O}{Q_S}+jQ_Oa \tag{20}$$

Similar to the case of the power factor, here also, only the variation of the minimum η_{coup} is analyzed. The maximum drops in efficiency varying with (Q_{in}, Q_O, L_{PR}) are shown in Fig. 4. The quality factors of the coupling coils, Q_r, Q_P, and Q_S, are set to 200 to calculate the efficiency, which are easy to achieve [18], [19]. Fig. 4 shows that the reduction of the transfer efficiency in most areas caused by compensation errors is less than 1%. Therefore, their effects can be ignored, and such parameters that Q_{in} is too small, and Q_O and L_{PR} are too large should be avoided during the design phase.

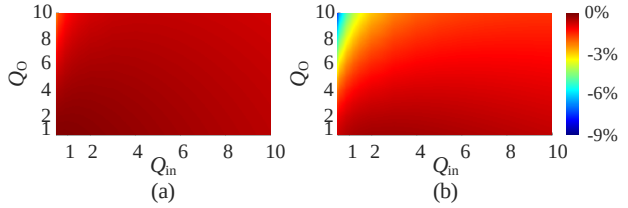

Fig. 4. Variation of the maximum drops in transfer efficiency η_{coup} with Q_{in}, Q_O, and L_{PR}. (a) L_{PR}=3. (b) L_{PR}=12.

4) *Voltages of Compensation Capacitors*

According to the circuit law, the currents through the capacitors will change sharply if the capacitors' terminal voltages change drastically, since the errors of the capacitors are smaller than ±10%. Therefore, only the changes in the capacitors' terminal voltages are studied here. With the same steps, the change ratios of three compensation capacitor voltages are derived and the primary parallel compensation capacitor's voltage is shown as follows:

$$\frac{U_{C_r}}{U_{C_{r-0}}} = \frac{1}{\left|(jQ_{in}-1)\left(1-k_r+\frac{1}{\frac{Q_{in}}{j-aQ_O}+b}\right)\right|} \tag{21}$$

Since the reduction of capacitor voltages will not affect circuit safety, only the variation of maximum voltages of compensation capacitors with (Q_{in}, Q_O, L_{PR}) is drawn in Fig. 5.

It can be found from Fig. 5 that the compensation errors have significant effects on the voltage of the primary parallel compensation capacitor. In some cases, the voltage increases

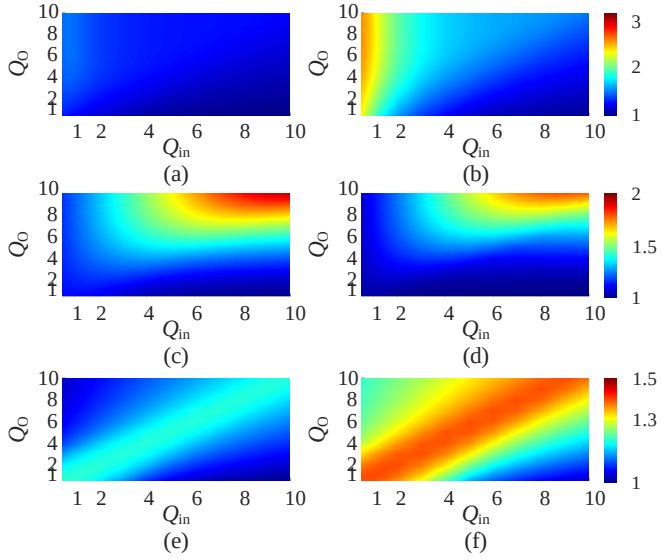

Fig. 5. Maximum ratios of the compensation capacitor voltages of detuned condition to that of ideal compensation condition varying with Q_{in}, Q_O, and L_{PR}. Primary parallel capacitor when (a) L_{PR}=3 and (b) L_{PR}=12. Primary series capacitor when (c) L_{PR}=3 and (d) L_{PR}=12. Secondary series capacitor when (e) L_{PR}=3 and (f) L_{PR}=12.

three times its normal value. Therefore, during the designing stage, the influence of the compensation errors on the electrical stress of the primary parallel compensation capacitor needs to be paid more attention, and that of the secondary compensation capacitor could be assigned less weight. Therefore, a higher Q_{in} and lower Q_O and L_{PR} are desired.

The above analysis shows that application of (Q_{in}, Q_O, L_{PR}) makes it easier to quantify the effect of capacitor errors on WPT systems. Under imperfect compensation conditions, the output voltage cannot be maintained at the expected value. With some parameters, the power factor may decrease significantly, leading to the need for a larger-capacity converter, which undoubtedly increases the cost. Besides, significant changes in capacitor voltages increase safety risks. Therefore, the WPT system designed with a traditional design strategy that does not consider the impacts of compensation errors may perform poorly in terms of reliability, safety, and cost. Moreover, the results show that it is very much possible to improve the detuning tolerance of WPT systems by designing (Q_{in}, Q_O, L_{PR}).

III. Design and Implementation of the WPT System with Improved Detuning Tolerance

A. *Design Requirements*

In this section, a design case of a 22-kW WPT charger, aiming at replacing the traditional wired charger for an electric bus, is discussed to verify the correctness of the above analysis. Tab.I summarizes the requirements defined by the user.

TABLE I
REQUIREMENTS OF THE DESIGN CASE

Indexes	Constrains
Coil size (mm^2)	< 1000 × 1000
Air gap (mm)	200
Output voltage change rates, ΔU_S	-30% < ΔU_S < +20%
Power factor, λ	>0.7
System transfer efficiency, η_{sys} (%)	> 90
Capacitor voltages change rates (%)	< +50

According to the previous analysis, the allowable ranges of (Q_{in}, Q_O, L_{PR}) could be obtained. Since Q_{in} is different, the allowed ranges of Q_O and L_{PR} will change, so their ranges are presented only when Q_{in} is equal to 0.5–7, as shown in Fig. 6.

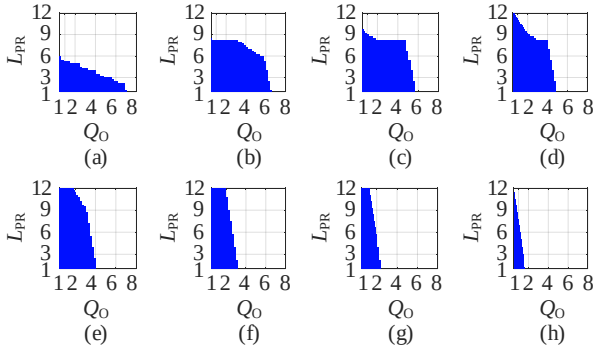

Fig. 6. Allowable ranges of Q_O and L_{PR} varying with Q_{in}. (a) Q_{in} =0.5. (b) Q_{in} =1. (c) Q_{in} =2. (d) Q_{in} =3. (e) Q_{in} =4. (f) Q_{in} =5. (g) Q_{in} =6. (g) Q_{in} =7.

Once the allowable ranges of these three parameters are obtained, the next step is to obtain the starting point for system design. The coupling coefficient could also be expressed by (Q_{in}, Q_O, L_{PR}), as shown below:

$$k = \frac{M}{\sqrt{L_P L_S}} = \sqrt{\frac{Q_{in}}{L_{PR} Q_O}} \tag{22}$$

It can be seen from the above equation that the larger the Q_{in} is, and the smaller the L_{PR} and Q_O are, the larger the k is, thus the more difficult the coil is to design. These three indicators, (Q_{in}, Q_O, L_{PR}), are not decoupled. As shown in Fig.6, when Q_{in} is different, the allowable ranges of Q_O and L_{PR} are also different. What is more, according to the theoretical analysis, (Q_{in}, Q_O, L_{PR}) have different or even contradictory effects on the system performance. For example, the increase in Q_{in} is beneficial to reduce $U_{\text{S\_Max}}$, but also reduces $U_{\text{S\_Min}}$, and a high Q_{in} reduces the increasing rates of the capacitor voltages. To obtain an option with good performance in all aspects, ($Q_{in\text{-}s}$, $Q_{O\text{-}s}$, $L_{PR\text{-}s}$) = (1, 5.5, 6), in which k equals 0.17, is manually selected as the design starting point. This coupling coefficient is easy to achieve and provides room for optimizing (Q_{in}, Q_O, L_{PR}). For this reason, the selected design point is close to but maybe not exactly the optimal point. A cost function with output voltage and other indexes considered is needed to determine an optimal design. However, the results will vary with the coefficients of each item in the cost function, and parameter sweeping is inevitable. The cost function is, therefore, not covered in this paper.

B. Parameters Design

At present, standard SAE J2954 presents the Test Station GA and VA specifications and some sample product GA and VA specifications for WPT1 (3.3 kW), WPT2 (7.7 kW) and WPT3 (11 kW). However, WPT4 (22 kW) and higher-power WPT systems are still in their early stages of definition [20]. Meantime, capacitor errors are not considered. This paper aims to develop a 22-kW wireless charger for an electric bus with high capacitor error tolerance. So, the coupling coils need to be designed, and their design process is introduced next.

Theoretically, there are an infinite number of combinations for coils, since many factors affect the performance of the coupling coils, such as the shape, size, and turns of the coil. Without a clear design process and guiding principles, system design requires continuous trial and error, which is quite cumbersome and places a huge burden on designers. Next, this paper will propose a simple and universal design process that can quickly get the compensation parameters and prototype of coupling coils meeting the aforementioned constraints.

The quality factor of the inverter can be rewritten when the parasitic resistances are ignored, as

$$Q_{in} = \frac{\omega M^2}{L_r R_E} = \frac{\omega L_r P_O}{U_P^2} \tag{23}$$

Once the input voltage and power level of the WPT system are determined, the compensation inductance can be determined first, about 17.9 μH, according to $Q_{in\text{-}s}$ suggested above and the recommended operating frequency of SAE J2954, 85 kHz. Then, the upper limit of the primary coil's self-inductance could be obtained according to $L_{PR\text{-}s}$, that is, $L_P \leq L_{PR\text{-}s}L_r$=107.7 μH, which provides the design constraint for the primary coil. If the self-inductance of obtained primary coil is smaller than 107.7 μH, then L_{PR} of the designed WPT system is smaller than $L_{PR\text{-}s}$, which is good for the system's detuning tolerance according to the previous analysis and Fig. 6.

Besides, once L_r is obtained, the mutual inductance M can be determined according to the voltage gain or output voltage requirements of the system. To fit the existed onboard DC-DC converter, the rated voltage gain is set to 1. So $M \geq 17.9$ μH needs to be satisfied. If the voltage gain and output power are known, then the upper limit of the self-inductance of the secondary coil can also be written,

$$L_S \leq \frac{Q_{O-s}U_P^2}{\omega P_O} = 98.7\mu\text{H} \tag{24}$$

As a result, with the constraints on (Q_{in}, Q_O, L_{PR}), the design process becomes to find the coupling coils whose mutual inductance is equal or very close, at least, to the target mutual inductance and self-inductances are lower than the upper limits. Therefore, the design of the primary and secondary coils is decoupled to some extent, and coupling coils with primary and secondary that are different in size and turns can be easily obtained without time-consuming parameters sweeping. This is the main advantage of the proposed design process. Since there are no calculation formulas for the coil design and it is expensive, time-consuming, and impractical to manufacture and test all possible coil combinations, the ANSYS simulation software is used here as an alternative. Trial and error with ANSYS and the use of empirical rules are inevitable, but it may only need a few tens of attempts to obtain expected coils.

Limited by the installation space, weight, and misalignment, the side length of the coil is limited from 400 to 1000 mm, with an increment of 100 mm, that is, the coil's side length is 400 mm, 500 mm, and so on. Square coils are selected due to their good anti-offset properties in all directions. PC95 magnetic core with a side length of the core laying area 100 mm longer than that of the coil area is used, which could help increase the quality factors of the coils [19]. A gap of 2 mm between adjacent turns is set to improve insulation and heat dissipation. The coil shape and core laying method can be optimized further, by using, for example, DD coils, which is beyond the scope of this paper. Fig. 7 shows the ANSYS model.

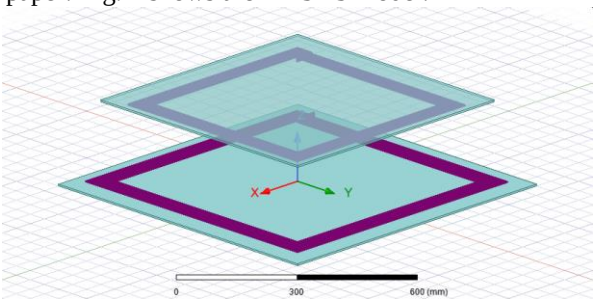

Fig. 7. ANSYS model.

The transfer efficiency is tested for all possible combinations obtained by simulations. To verify whether the system efficiency requirements are met, it is assumed that the efficiency of the primary converter is 98%, including a three-phase rectifier and a high-frequency inverter, and that of the secondary rectifier is 99%. These assumptions are reasonable according to the published literatures [10], [11], [21], [22]. If the quality factors of the actual coils are greater than 200 or the efficiency of converters are higher than the assumptions, the transfer efficiency will be higher under the same working conditions.

If the coil design constrains or system requirements are not satisfied, then Q_{in} should be changed and the above design process should be repeated. The summarized design process is shown in Fig. 8, and the optional coils obtained with the proposed design process are shown in Tab.II.

It should be noted that at least two of the three parameters of

TABLE II
PARAMETERS OF THE COILS OBTAINED WITH THE PROPOSED DESIGN PROCESS

Primary		Secondary		L_P(μH)	L_S (μH)	M (μH)	k	Q_{in}	Q_O	L_{PR}	η_{sys} (%)	$\frac{\Delta M}{M}$ (%)
Turns	Length(mm)	Turns	Length(mm)									
4	700	5	800	51.4	86.7	16.7	0.251	0.93	4.83	3.07	92.73%	-14.24%
4	700	6	700	49.5	97.9	18.0	0.258	1.00	5.45	2.75	92.67%	-15.44%
4	700	7	600	50.3	104.5	16.8	0.232	0.94	5.82	2.99	92.33%	-15.32%
4	800	5	800	60.4	88.5	19.7	0.270	1.10	4.93	3.06	92.85%	-15.38%
4	800	5	900	61.2	100.8	21.0	0.268	1.17	5.62	2.91	92.64%	-13.03%
4	800	6	700	57.7	99.0	19.1	0.253	1.07	5.52	3.01	92.58%	-11.97%
4	900	5	800	68.6	89.6	20.7	0.264	1.15	4.99	3.31	92.75%	-13.74%

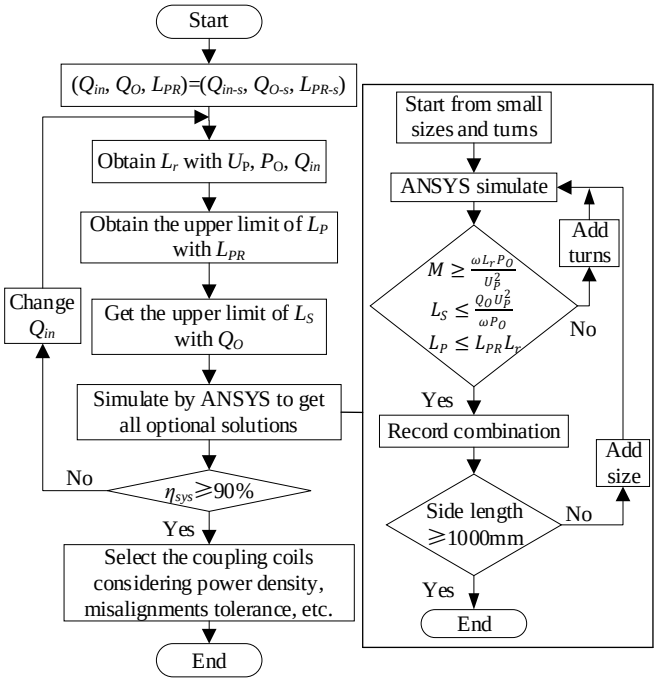

Fig. 8. Proposed design process.

the coupling coils, L_P, L_S, and M, will change simultaneously when any parameter of the turns and dimensions of the primary and secondary coils changes, resulting in at least two of (Q_{in}, Q_O, L_{PR}) changed. To prevent possible options from being missed, the coupling coils that do not meet but are close to the restrictions are also checked.

There may be offsets between the primary and secondary coils in practice, which will cause changes in the transfer characteristics of the system. So, the ANSYS models are also simulated when offsets in the *X*- and *Y*- direction are both maximum, 75 and 100 mm, respectively, and the mutual inductance is obtained. There is no *Z*-direction offset requirement from the user, so the air gap is set to 200 mm and kept constant. The drop rates of mutual inductance compared with aligned conditions, $\Delta M/M$, are used to evaluate the misalignment tolerance and listed in the last column in Tab.II.

Since the transfer efficiency of these combinations is similar and satisfies the requirements, misalignment tolerance and power density are also considered when the indicated design is selected. The combination, primary 4 turns with 800 mm and secondary 6 turns with 700 mm, is finally selected as it has good performance in all these aspects.

C. Simulation Performance Compared to a Traditional Design Method

It is a difficult task to design primary and secondary coils with different parameters considering various influencing factors without clear guidelines as many factors affect the coils' performance. So traditionally, some coupling-related variables are often fixed, and only some other variables are optimized to simplify the system design. Identically same primary and secondary coil combinations were adopted in many literatures [10]–[16]. Here, the primary and secondary coils are also set to the same.

The design of the compared case is based on some rules of thumb: a) the more turns and the larger the size, the greater the coupling coefficient is; b) the larger the coupling coefficient, the greater the transfer efficiency is [19]. Since capacitor errors are not considered, the output voltage and other indicators are considered to keep as rated values. The transfer efficiency becomes the only design target. When the coils are designed, this target is transformed into making the coupling coefficient as large as possible. In terms of constraints, a practical constraint is that Q_O should be smaller than 10 to avoid too high capacitor voltages [23]. The voltage of the secondary series capacitor is the highest among these three capacitors, in general, so limiting Q_O alone is enough. For fair comparison, the voltage gain is also set to 1. The same fixed coupling-related variables are applied. That is, the same sizes and layout method of magnetic core are used. The parameters to be designed are also the turns and size. With the trial-and-error method for ANSYS simulation to find the coupling coils with high coupling coefficient, optional coils are obtained, as shown in Tab. III. The coupling coils with 7 turns and 800 mm long are chosen to achieve a balance between the coupling coefficient, misalignment tolerance, and power density.

TABLE III
PARAMETERS OF THE COILS OBTAINED WITH TRADITIONAL METHOD

Turns	Length (mm)	L_P(μH)	L_S(μH)	M (μH)	k	$\frac{\Delta M}{M}$ (%)
6	1000	157.8	157.8	51.5	0.326	-13.19%
7	800	152.1	152.2	46.9	0.308	-14.08%
7	900	178.4	178.6	58.3	0.326	-12.88%
8	700	156.1	156.2	46.4	0.297	-15.42%
10	600	174.4	173.3	49.8	0.287	-19.27%

Tab.IV compares the results obtained with the proposed design process and the traditional method.

IV. VERIFICATION EXPERIMENTS

A. Experimental Platform

To verify the correctness of the previous theoretical analysis, experiments were carried out on a 30-kW platform, as shown in Fig. 9. The actual rated power level was set to 22 kW with the input voltage 380 V, 50 Hz to ensure safety, as the output voltage may be higher than the rated value. To maintain the consistency of the input voltage and the load, a three-phase programmable AC power supply was used as the input. A

TABLE IV
PARAMETERS OF THE OBTAINED EXAMPLES

Parameters	Optimized Example	Compared Example
Primary	4 turns, 800 mm	7 turns, 800 mm
Secondary	6 turns, 700 mm	7 turns, 800 mm
Q_{in}	1.07	2.62
Qo	5.52	8.48
L_{PR}	3.01	3.24
Maximum and minimum change ratios (ΔU_S)	+13.4%/-27.5%	13.6%/-42.8%
Minimum power factor	0.77	0.62
Maximum increasing ratios of U_{C_r}, U_{C_P}, U_{C_S}	48.3%/27.1%/ 17.8%	36.9%/39.1%/ 18.5%
Maximum drop in η_{coup}	-0.8%	-1.0%

Chroma 17040 battery simulator was used as the load and was operated in constant resistance (CR) discharge mode, whose resistance was set to 11.8 Ω and corresponded to the rated output power of 22 kW under perfect compensation condition.

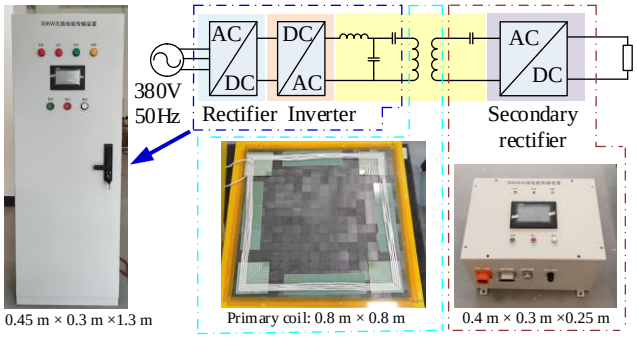

Fig. 9. Experimental platform.

Litz wire was used to wind coils, which was 7 mm in diameter and had 2200 strands with 0.1-mm diameter. A Microtest 6630 LCR meter was used to measure coils' self-inductance, mutual inductance, and capacitances. The coil parameters of the optimized example and the compared case are shown in Tab.V.

TABLE V
PARAMETERS OF THE COILS

	Optimized Example			Compared Example		
	Sim(μH)	Mea(μH)	Error	Sim(μH)	Mea(μH)	Error
L_P	57.7	61.3	5.9%	152.1	156.0	2.5%
L_S	99.0	100.1	1.1%	152.2	153.9	1.1%
M	19.1	20.7	7.7%	46.9	49.6	5.4%

According to Tab.III, the errors between simulation and actual winding were not more than 7.7%, which were acceptable. The (Q_{in}, Q_O, L_{PR}) of the optimized example and compared case were (1.16, 5.58, 3.20) and (2.77, 8.58, 3.15).

The ideal and worst compensated conditions for the optimized example and compared one were performed, respectively. The experiments when the maximum horizontal offset occurred with ideal compensation were also implemented to compare the impacts of capacitor errors and misalignments on the system. The values of (C_r, C_P, C_S) in experiments are listed in Tab.VI and the data in brackets are theoretical (k_r, k_P, k_S). Due to the limited number of compensation capacitors and the discontinuous capacitance values, there were errors between the expected capacitances and actual capacitances in experiments. For instance, the maximum output voltage occurred at (k_r, k_P, k_S) = (1.1, 1.1, 0.977), and the corresponding compensation capacitors (C_r, C_P, C_S) = (186.4 nF, 94.8 nF, 34.2 nF), whereas the actual capacitances were (186.6 nF, 95.0 nF, 34.2 nF). However, the errors between the actual and ideal values were very small and could be considered as the expected values.

TABLE VI
CAPACITANCES IN EXPERIMENTS

Experimental Condition	C_r, C_P, C_S (nF) of Optimized Example	C_r, C_P, C_S (nF) of Compared Example
Ideal compensation	169.6, 85.9, 35.0	70.5, 32.9, 22.8
Maximum output voltage	186.6, 95.0, 34.2 (1.1, 1.1, 0.977)	77.5, 36.4, 22.0 (1.1, 1.1, 0.965)
Minimum output voltage	152.8, 95.0, 31.4 (0.9, 1.1, 0.9)	66.3, 36.4, 20.4 (0.9, 1.1, 0.9)
Minimum power factor	165.7, 94.9, 30.8 (0.975, 1.1, 0.9)	66.3, 36.4, 20.4 (0.9, 1.1, 0.9)
Maximum U_{C_r}	186.6, 95.0, 31.5 (1.1, 1.1, 0.9)	77.5, 36.4, 21.1 (1.1, 1.1, 0.929)
Maximum U_{C_P}	186.6, 77.5, 31.5 (1.1, 0.9, 0.9)	77.5, 29.6, 20.4 (1.1, 0.9, 0.9)
Maximum U_{C_S}	186.6, 95.0, 33.2 (1.1, 1.1, 0.948)	77.5, 36.4, 21.5 (1.1, 1.1, 0.953)

Tektronix current probes were used to measure the currents of capacitors during the experiments, and the compensation capacitor voltages were calculated from the capacitances and the currents. The system transfer efficiency was measured from the primary three-phase input to the secondary rectifier output by a Tektronix PA3000 power analyzer.

B. Experiments Results

Some waveforms of the voltages and currents are shown in Fig.10.

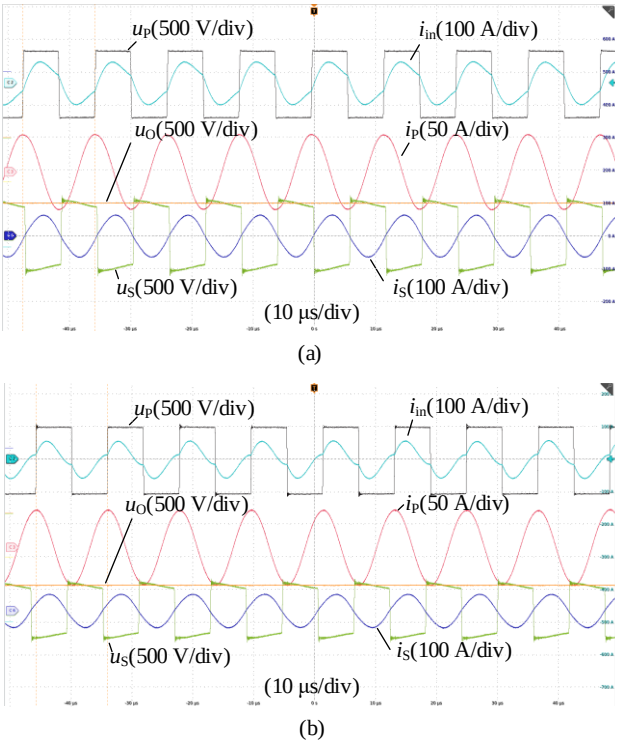

Fig. 10. Experimental waveforms of voltages and currents. (a) Optimized example, aligned with ideal compensation. (b) Optimized example, aligned with minimum output voltage.

From Fig. 10(a) and (b), when capacitors had errors, the output voltage was reduced from 495.2 V to a minimum value

of 389.0 V, with a drop rate of 21.5%. Besides, the inverter output current was distorted, and the system was capacitive for the inverter output, which would adversely affect the transfer efficiency of the system.

The experimental results are displayed in Tab.VII. The output voltage, power factor, capacitor voltages, and transfer efficiency of the system are listed for aligned conditions with ideal compensation. For the aligned condition with worst compensation and misaligned condition, the output voltages and capacitor voltages are presented as the change ratios compared with the ideal compensated and aligned condition, whereas the power factor and transfer efficiency are still measurement results. The variation in transfer efficiency η_{coup} caused by capacitor errors could be ignored theoretically, so it is not taken into consideration when the coupling coils are designed. The transfer efficiency of worst compensation is the minimum one among the seven compensation conditions listed in Tab.IV.

TABLE VII
EXPERIMENTAL RESULTS

Index	Optimized example			Compared example		
	Aligned		Misaligned	Aligned		Misaligned
	Ideal	Worst		Ideal	Worst	
U_S	495.4 V	12.4% -21.5%	-11.6%	485.9 V	13.1% -40.9%	-13.8%
λ	0.99	0.78	0.99	1	0.64	1
U_{C_r}	700.7 V	48.3%	-12.6%	1289.6 V	40.3%	-23.2%
U_{C_P}	890.5 V	27.7%	1.0%	955.2 V	42.7%	1.1%
U_{C_S}	2460.0 V	20.0%	-11.4%	3940.2 V	12.0%	-19.3%
η_{sys}	93.2%	87.3%	92.8%	91.3%	81.4%	91.4%

Since the converter losses, coil resistances, and so on are not considered in the theoretical analysis, the experimental results are somewhat different from the theoretical calculations. For instance, the output voltage of perfect compensation condition was less than 510 V. However, the overall error was acceptable, which was less than 5%, except for efficiency. The theoretical calculation ignores the changes in converter loss with compensation errors. When the compensation errors exist, the power factor is usually less than 1, which will cause the primary inverter's current to increase, resulting in a large change in system efficiency. What is more, the compared example has a larger coupling coefficient but a lower system transfer efficiency. This is caused by the fact that the quality factors, Q_r, Q_P, and Q_S, will vary with the turns and sizes of the actual coils, rather than keeping as constant values. The loss of capacitors is theoretically ignored, which will also affect the system efficiency.

When the results of the optimized example were compared with that of the compared case, although the increasing ratios of voltages of C_r and C_S, $U_{C_r}/U_{C_{r-0}}$ and $U_{C_S}/U_{C_{S-0}}$, of the optimized case were greater than those of the compared case, the overall difference was not much and no more than 8%. However, compensation errors cause that the compared case may output a lower voltage. The minimum was as low as 289.0 V, which was about half the maximum value, while the drop rate of the optimized example was only 21.5%. The maximum rising ratio of the output voltage of the proposed design was 0.7 % smaller than that of the traditional design. For the power factor, the minimum value for the optimized case was about 0.78, that is, 0.14 greater than that of the compared case. Therefore, the traditional design needs a larger-capacity converter, which obviously results in an increase in cost. Although, in theory, the transfer efficiency is not sensitive to the compensation errors, the experimental results show that the compensation errors do have some impacts. The efficiency of the compared case was more affected, varying from 91.3% to 81.4%, whereas the maximum drop was only 5.9% for the proposed design. This is because the minimum output voltage and minimum power factor of the optimized case are larger, that is, the optimized case is less affected compared with the compared example.

Between misalignment and capacitor errors, capacitor errors have a greater influence. For the optimized example, the output voltage was reduced from 495.4 to 437.2 V when the maximum offsets occurred, with a drop rate of 11.6%. This was consistent with the simulated mutual inductance drop of 11.97%. However, when capacitor errors were ±10%, the output voltage dropped even more, as low as 21.5%. Besides, when the output voltage was minimum, the inverter output current was distorted and the system was capacitive for the inverter output. Capacitor errors caused the power factor to decrease with a minimum value of 0.78, while misalignment alone had almost no effect on the power factor. In addition, misalignment usually decreases capacitor voltages, whereas capacitor errors may cause their voltages to increase, with U_{C_r} increasing by as much as 48.3%. In terms of transfer efficiency, the drop in efficiency caused by misalignment was negligible, only 0.4%, compared with 5.9% of detuning condition. So, compared with the capacitor errors, misalignment has less influence on the system. The same conclusion can be obtained from the compared case as well. The reason is that only one parameter, mutual inductance, changes significantly when the offsets occur. However, there are three compensation capacitors. Although the error of each capacitor is ±10%, the effect is amplified by the combination of specific parameters compared to the case where only one capacitor error is considered.

The output voltage of the proposed design dropped less with misalignment, only 11.6%, whereas the compared case had 13.8%. The capacitor voltages of the proposed case dropped less too. Therefore, the proposed design has better misalignment tolerance. This is because the primary coil is larger than the secondary coil, whereas they are same for the conventional design. Although the transfer efficiency of the optimized case was reduced, it was only 0.4%, which was negligible. The difference in efficiency is due to different coil parameters resulting in different efficiency versus load curves.

V. CONCLUSION

In this article, the effect of capacitor errors on transfer characteristics was analyzed in detail, and a simple and easy-to-follow design process of the coupling coils with improved capacitor error tolerance was proposed. The primary quality factor Q_{in}, load quality factor Q_O, and the ratio of the primary coil's self-inductance to the compensation inductance L_{PR} were used to express the transfer characteristics, which simplified the analysis of the relationships among the output voltage, power factor, transfer efficiency, and capacitor voltages with parameters of coils, and capacitor errors. To comprehensively evaluate the impacts of the capacitor errors on

the system, the situation in which the three capacitors of the LCC-S circuit were simultaneously in error was considered, which was consistent with the actual application. With the proposed design process, the coupling coils satisfying the design requirements, with (Q_{in}, Q_O, L_{PR}) equal to (1.07, 5.52, 3.01), were easily found. Experiments carried out on a 22-kW platform with an air gap of 200 mm verified the correctness of theoretical analysis and the effectiveness of the proposed design process in improving the capacitor error tolerance. Experimental results show that the change ratio of the output voltage of the proposed design was between -21.5% and 12.4%, while that of the conventional design was between -40.9% and 13.1%. The power factor was always greater than 0.78 and the drop in efficiency was no more than 5.9%, while the minimum power factor and maximum drop in efficiency of the conventional design were 0.64 and 9.9%, respectively.

REFERENCES

[1] H. Feng, R. Tavakoli, O. C. Onar and Z. Pantic, "Advances in high-power wireless charging systems: overview and design considerations," *IEEE Trans. Transport. Electrific.*, vol. 6, no. 3, pp. 886-919, Sept. 2020.

[2] H. Oh *et al*., "6.78 MHz wireless power transmitter based on a reconfigurable class–E power amplifier for multiple device charging," *IEEE Trans. Power Electron*., vol. 35, no. 6, pp. 5907-5917, June 2020.

[3] S. Lee et al., "Voltage-boosted current-mode wireless power receiver for directly charging a low-voltage battery in implantable medical systems," *IEEE Trans. Ind. Electron*., vol. 66, no. 11, pp. 8860-8865, Nov. 2019.

[4] V. X. Thai, G. C. Jang, S. Y. Jeong, J. H. Park, Y. -S. Kim and C. T. Rim, "Symmetric sensing coil design for the blind-zone free metal object detection of a stationary wireless electric vehicles charger," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3466-3477, April 2020.

[5] J. T. Boys, G. A. Covic, and A. W. Green, "Stability and control of inductively coupled power transfer systems," *Proc. IEE—Elect. Power Applicat*., vol. 147, no. 1, pp. 37–43, Jan. 2000.

[6] *Film capacitors—Metallized polypropylene film capacitors (MKP)*, TDK, Tokyo, Japan, 2019.

[7] Y. Wang, Y. Yao, X. Liu, D. Xu and L. Cai, "An LC/S compensation topology and coil design technique for wireless power transfer," *IEEE Trans. Power Electron*., vol. 33, no. 3, pp. 2007-2025, March 2018.

[8] H. Zhang and F. Lu, "An improved design methodology of the double-sided LC-compensated CPT system considering the inductance detuning," *IEEE Trans. Power Electron.*, vol. 34, no. 11, pp. 11396-11406, Nov. 2019.

[9] F. Lu, H. Hofmann, J. Deng, and C. Mi, "Output power and efficiency sensitivity to circuit parameter variations in double-sided LCC-compensated wireless power transfer system," *Proc. IEEE Appl. Power Electr. Conf.*, 2015, pp. 597–601.

[10] R. Bosshard and J. W. Kolar, "Multi-objective optimization of 50 kW/85 kHz IPT system for public transport," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 4, pp. 1370–1382, Dec. 2016.

[11] R. Bosshard, U. Iruretagoyena and J. W. Kolar, "Comprehensive evaluation of rectangular and double-D coil geometry for 50 kW/85 kHz IPT system," *IEEE J. Emerg. Sel. Topics Power Electron*, vol. 4, no. 4, pp. 1406-1415, Dec. 2016.

[12] M. Budhia, G. A. Covic and J. T. Boys, "Design and optimization of circular magnetic structures for lumped inductive power transfer systems," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3096-3108, Nov. 2011.

[13] M. Budhia, J. T. Boys, G. A. Covic and C. Huang, "Development of a single-sided flux magnetic coupler for electric vehicle IPT charging systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 1, pp. 318-328, Jan. 2013.

[14] M. Lu and K. D. T. Ngo, "Systematic design of coils in series–series inductive power transfer for power transferability and efficiency," *IEEE Trans. Power Electron*., vol. 33, no. 4, pp. 3333-3345, April 2018.

[15] A. Delgado, D. Schoenberger, J. Á. Oliver, P. Alou and J. A. Cobos, "Design guidelines of inductive coils using a polymer bonded magnetic composite for inductive power transfer systems in electric vehicles," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 7884-7893, Aug. 2020.

[16] A. Ramezani, S. Farhangi, H. Iman-Eini, B. Farhangi, R. Rahimi and G. R. Moradi, "Optimized LCC-series compensated resonant network for stationary wireless EV chargers," *IEEE Trans. Ind. Electron.*, vol. 66, no. 4, pp. 2756-2765, April 2019.

[17] Y. Geng, Z. Yang and F. Lin, "Design and control for catenary charged light rail vehicle based on wireless power transfer and hybrid energy storage system," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 7894-7903, Aug. 2020.

[18] W. Zhang, J. C. White, A. M. Abraham and C. C. Mi, "Loosely coupled transformer structure and interoperability study for EV wireless charging systems," *IEEE Trans. Power Electron*., vol. 30, no. 11, pp. 6356-6367, Nov. 2015.

[19] F. Y. Lin, G. A. Covic and J. T. Boys, "Evaluation of magnetic pad sizes and topologies for electric vehicle charging," *IEEE Trans. Power Electron*., vol. 30, no. 11, pp. 6391-6407, Nov. 2015.

[20] SAE international, "Wireless power transfer for light-duty plug-in/electric vehicles and alignment methodology," 2020. [Online] Available: https://www.sae.org/standards/content/J2954_202010.

[21] V. P. Galigekere *et al.*, "Design and implementation of an optimized 100 kW stationary wireless charging system for EV battery recharging," *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Portland, OR, Sep. 2018, pp. 3587–3592.

[22] *ORNL demonstrates 120-Kilowatt wireless charging for vehicles*. Accessed: Oct. 19, 2018. [Online]. Available: https://www.ornl.gov/news/ornl-demonstrates-120-kilowatt-wireless-charging-vehicles

[23] M. G. S. Pearce, G. A. Covic and J. T. Boys, "Robust ferrite-less double D topology for roadway IPT applications," *IEEE Trans. Power Electron*., vol. 34, no. 7, pp. 6062-6075, July 2019.

Yi Wang (M'18) received the B.S. degree from China University of Mining & Technology-Beijing, Beijing, China, in 2016; the M.S. degree in Beijing Jiaotong University, Beijing, China, in 2019, where he is currently working toward the Ph.D degree with the School of Electrical Engineering, all in electrical engineering.

His research interests include power electronics and wireless power transfer technology.

Zhongping Yang (M'14) received the B.Eng. degree from Tokyo University of Mercantile Marine, Tokyo, Japan, in 1997 and the M.Eng. and Ph.D. degrees from the University of Tokyo, Tokyo, Japan, in 1999 and 2002, respectively, all in electrical engineering.

He is currently a Professor with the School of Electrical Engineering, Beijing Jiaotong University, Beijing, China. His research interests include high-speed rail integration technology, traction and regenerative braking technology, and wireless power transfer of urban rail vehicles.

Prof. Yang received the Zhan Tianyou Award for Science and Technology in 2010, the Excellent Popular Science and Technology Book Award in 2011, and the Science and Technology Progress Award (second prize) of Ministry of Education in China in 2016.

Fei Lin (M'05) received the B.S. degree from Xi'an Jiaotong University, Xi'an, China; the M.S. degree from Shandong University, Jinan, China; and the Ph.D. degree from Tsinghua University, Beijing, China, in 1997, 2000, and 2004, respectively, all in electrical engineering.

He is currently a Professor with the School of Electrical Engineering, Beijing Jiaotong University. His research interests include traction converters and motor drives, energy management for railway systems, and digital control of power-electronic-based devices.